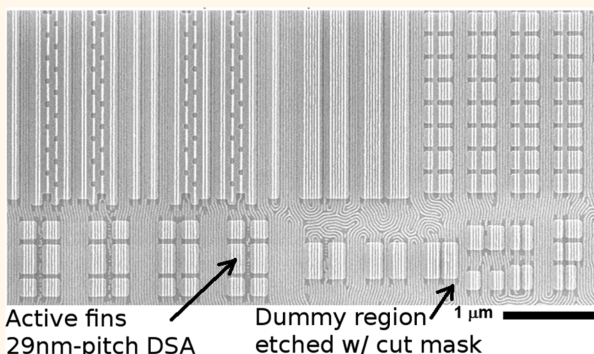
Two-Dimensional Pattern Formation Using Graphoepitaxy of PS-*b*-PMMA Block Copolymers for Advanced FinFET Device and Circuit Fabrication

Hsinyu Tsai,[†,*] Jed W. Pitera,[‡] Hiroyuki Miyazoe,[†] Sarunya Bangsaruntip,[†] Sebastian U. Engelmann,[†] Chi-Chun Liu,[§] Joy Y. Cheng,[‡] James J. Bucchignano,[†] David P. Klaus,[†] Eric A. Joseph,[†] Daniel P. Sanders,[‡] Matthew E. Colburn,[§] and Michael A. Guillorn[†]

[†]IBM Watson Research Center, 1101 Kitchawan Road, Yorktown Heights, New York 10598, United States, [‡]IBM Research Almaden, 650 Harry Road, San Jose, California 95120, United States, and [§]IBM Albany Nanotech Research Center, 257 Fuller Road, Albany, New York 12203, United States

ABSTRACT Directed self-assembly (DSA) of lamellar phase block-*co*-polymers (BCPs) can be used to form nanoscale line-space patterns. However, exploiting the potential of this process for circuit relevant patterning continues to be a major challenge. In this work, we propose a way to impart two-dimensional pattern information in graphoepitaxy-based lamellar phase DSA processes by utilizing the interactions of the BCP with the template pattern. The image formation mechanism is explained through the use of Monte Carlo simulations. Circuit patterns consisting of the active region of Si FinFET transistors, referred to as Si "fins", were fabricated to demonstrate the applicability of this technique to the formation of complex patterns. The quality of the Si fin features produced by this process was validated by demonstrating the first functional DSA-patterned FinFET devices with 29 nm-pitch fins.



KEYWORDS: block copolymer · directed self-assembly · graphoepitaxy · FinFET scaling

Progress in advanced CMOS technology is increasingly reliant on a complex blend of device, interconnect, patterning and circuit design innovation. Breakthroughs in one of these areas can often drive the others forward at an unexpected pace. An example of this can be found by examining the move from conventional MOSFETs to the FinFET transistor. A FinFET is composed of an ensemble of discrete single crystal Si mesas or "fins" having widths on the order of 10 nm and heights in the 20–40 nm range. The raised geometry of the fin allows the gate electrode to wrap around the body of the device providing improved control over the fields in the channel. Compared to conventional MOSFETs where the gate can only apply a field to one side of the channel, the FinFET shows better performance at smaller gate lengths. This advantage has driven the semiconductor industry to move toward FinFET-based device technology starting at the 22 nm process node.[1]

The spatial frequency, or pitch, of the fins is an integral part of FinFET device and circuit design. The impact of fin pitch on layout density is obvious. Denser fin pitch also leads to a reduction in parasitic capacitance and, consequently, lower power or higher operating speed.[2] Identifying an optimal fin pitch ultimately must balance design and performance considerations with process technology reality. High-resolution, high-throughput photolithography is currently limited to a pitch resolution of ~80 nm. However, a fin pitch of 60 nm produced by a sublithographic pitch reduction technique was used for 22 nm node FinFETs.[1] This fin pitch was selected because it offered a more optimal choice for device and circuit performance compared

* Address correspondence to htsai@us.ibm.com.

Received for review March 5, 2014 and accepted March 26, 2014.

Published online March 26, 2014
10.1021/nn501300b

© 2014 American Chemical Society

to an 80 nm fin pitch, which would have arguably been a more predictable decision. This advance in effective pitch resolution marks the first time sublithographic patterning has been used in a high performance logic technology. Even ignoring effects on yield, the use of sublithographic pitch reduction increases process complexity and, in turn, elevates production cost. Regardless, this was a step the semiconductor industry was willing to take in order to maximize the potential benefit of FinFET transistors.

Scaling of the fin pitch below 60 nm will be required in future process nodes. Demonstrations of FinFET devices and circuits suitable for the 14 nm node have been reported by sublithographic halving of the minimum pitch of 193 nm based photolithography resulting in a 40 nm fin pitch. Moving beyond this design point will either require a reduction in the minimum lithographic resolution or a further innovation in sublithographic patterning technology. For this reason, the concept of forming line-space patterns by directed self-assembly (DSA) of block copolymers (BCPs) has received a significant amount of attention in recent years. DSA of BCPs has been shown to result in pitch reduction of lithographically printed template patterns with reports of minimum feature pitches below 20 nm.[3,4] Early work by C. Black and co-workers demonstrated a FinFET-like transistor with a 40 nm fin pitch patterned by DSA.[5] The fin patterns were formed using a one-dimensional graphoepitaxy-based self-assembly process with rectangular trenches in various substrates.[6] In spite of these promising results, further work on FinFET transistor fabrication using DSA has yet to be published. This is in part due to the complexity associated with turning the regular features formed by DSA into the type of pattern constructs required for scaled FinFET devices and circuits.

In this work, we demonstrate a way to impart two-dimensional (2D) pattern information in graphoepitaxy-based lamellar phase line-space DSA processes. This is accomplished by exploiting the interactions of the BCP with the template pattern and the introduction of limited 2D geometry in the template design. DSA is then performed using a poly(styrene-*block*-methyl methacrylate) (PS-*b*-PMMA) BCP with a natural length, Lo, of 29 nm. 2D self-assembly with PS-*b*-PMMA in a graphoepitaxy-based process was previously shown to form a limited set of complex structures, such as bent vertical lamellar domains and concentric vertical cylindrical domains.[7] However, the image formation mechanism was not studied. In this paper, we apply Monte Carlo simulations of the self-assembly process to reveal how 2D patterns can be directly formed in the PMMA phase of a PS-*b*-PMMA BCP. Using plasma etching to remove the PMMA phase followed by a tone inversion process, we demonstrate that this image can be used to produce raised Si features suitable for FinFET device fabrication. The resulting patterns can be further customized by conventional lithographic and etching techniques to form patterns well suited for FinFET logic and memory circuits. We illustrate the concept by demonstrating the synthesis of example circuit patterns including the

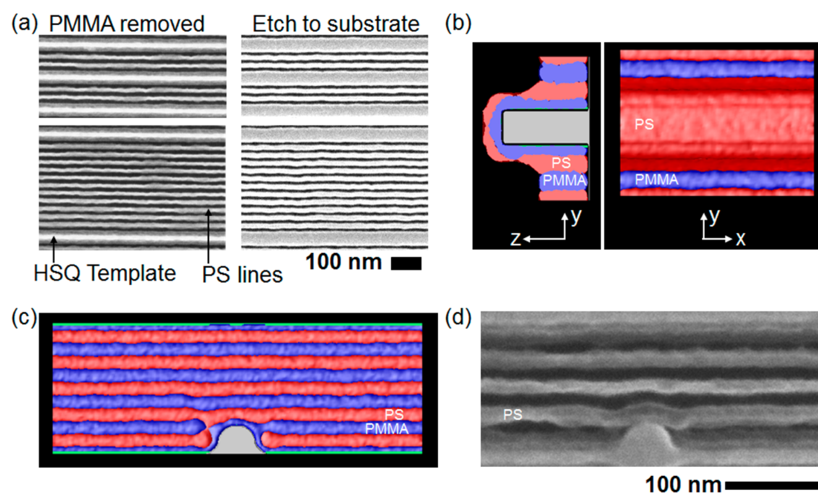


Figure 1. In DSA graphoepitaxy, interaction between guiding patterns and the preferred polymer domain provides unique capabilities for self-aligned customization. Using PS-*b*-PMMA graphoepitaxy with HSQ guiding patterns as an example, we found two interesting phenomena: (a) PMMA half-domains adjacent to HSQ lines do not participate in pattern transfer into subsequent hard mask layers during reactive ion etch, resulting in only full PMMA domains being transferred. (b) Monte Carlo simulations show that the PMMA half domains can be protected by their adjacent PS half domain when there is a ~0.5Lo thick surface layer around guiding lines. When introducing certain two-dimensional structures into the guiding pattern, one can cleanly truncate a PMMA domain. Simulations confirmed the feasibility of this type of two-dimensional graphoepitaxy with a preferred line-space orientation. If we use the PMMA phase for image formation, we can now form complex two-dimensional patterns with self-aligned customization. (c) Monte Carlo simulation and (d) an experimental example showing how PS-*b*-PMMA interacts with HSQ templates when there are two-dimensional structures on the template. The PMMA domains are partially etched to improve image contrast. The brightest lines correspond to the HSQ template, the darkest lines correspond to etched PMMA domains, and the lines in the middle are the remaining PS domains.

demonstration of functioning DSA-patterned FinFET transistors with a fin pitch of 29 nm.

RESULTS AND DISCUSSION

In DSA graphoepitaxy, the topography of the substrate registers and orients the BCP microdomains. For graphoepitaxy with lamellar BCP, the sidewalls of the template patterns preferentially interact with one domain of the BCP while the bottom surface is kept chemically neutral allowing lamellar line-space patterns to form parallel to the sidewalls of the template. Figure 1a shows an example using PS-*b*-PMMA graphoepitaxy with SiO_x guiding patterns formed by electron beam lithography of hydrogen silsesquioxane

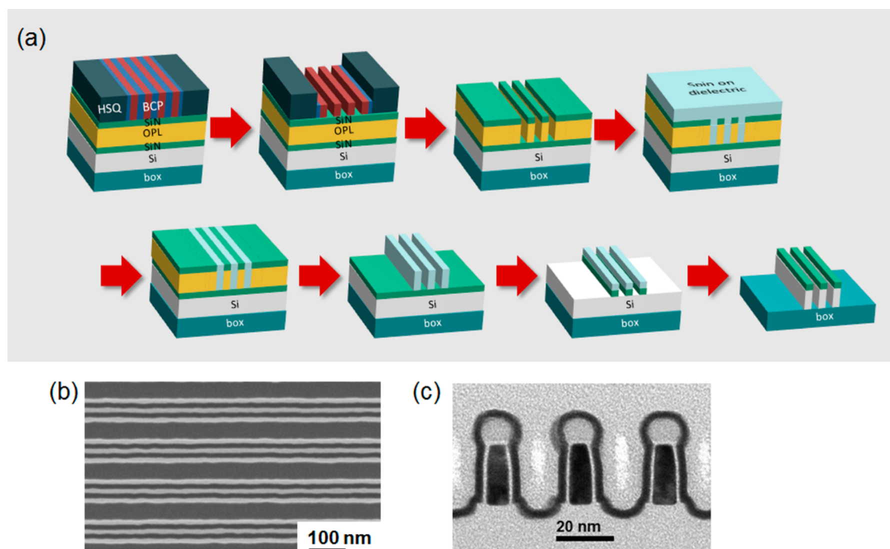


Figure 2. Fin formation using patterns from the PMMA-phase. (a) Process flow for forming groups of silicon on insulator (SOI) fins with a controlled fin spacing. A tone inversion operation is applied after etch transferring the DSA pattern into an organic planarizing layer (OPL). The tone inverted image is then transferred into a fin hard mask layer and 20 nm of SOI. (b) A top down scanning electron microscope (SEM) image of a group of fins formed with the process shown in (a). The space between groups of fins is defined by the DSA guiding pattern. (c) A transmission electron microscope (TEM) image of 29 nm pitch SOI fins formed with the process shown in (a).

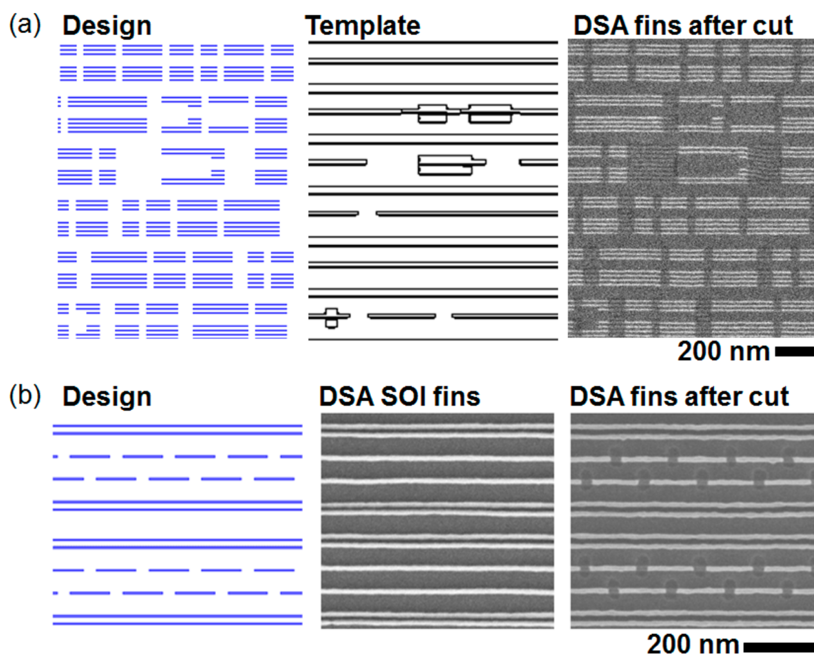


Figure 3. Fin circuit demonstrations with DSA-patterned fins. (a) Logic and (b) SRAM fin patterning example showing the fin design, template design, and fins after etch transfer into SOI.[8] Several highly desirable features for FinFET circuit design are demonstrated in this example, including the formation of group of 2–4 fins and a 1–2 fin transition between different numbers of fins. When DSA graphoepitaxy templates are used as the self-aligned cut mask between groups of fins, partial fin removal due to misalignment of the hard mask can be completely avoided. A second, less critical cut mask is used to generate fin breaks along the groups of fins. The pitch of all dense lines is 29 nm.

resist (HSQ). Electron beam irradiation converts HSQ into a low quality SiO_x. These SiO_x features preferentially attract PMMA domains. It is expected that the number of PS domains can be modulated by adjusting the spacing between two adjacent template features. However, we found two interesting phenomena by more carefully examining the DSA behavior at the template pattern sidewalls. First, the PMMA half-domains adjacent to HSQ features unexpectedly were not revealed after exposure to an RIE process designed to selectively remove the PMMA phase.[7] Consequently, only full PMMA domains participated in further pattern transfer. This also creates an unpatterned region between two groups of full PMMA phases that is the combined width of the template feature, the half PMMA phases on either side of the template and the full PS phases adjacent to the half PMMA phases. The second surprising phenomenon we discovered was that the introduction of 2D geometry in the guiding pattern can cleanly truncate PMMA domains perpendicular to the guiding pattern sidewall. This provides a way to terminate a limited number of lines in a group while allowing others to run continuously over longer distances. Moreover, the position of the line ends is aligned to the template sidewall.

Monte Carlo simulations are a valuable tool for understanding the behavior of BCPs during the DSA process. Three-dimensional (3D) simulations of DSA conducted in the presence of a template pattern show that the PMMA half domains adjacent to the sidewall can be wrapped by their adjacent PS half domain if there is an ~0.5Lo thick surface wetting layer of BCP over the guide pattern. This is shown in Figure 1a,b. The physical situation required to produce this result can be engineered by choosing a template material with proper chemical affinity to PMMA, the correct template height, and BCP thickness. Further simulations of 2D template geometries confirmed that the truncation of the PMMA phase arises from a dislocation-like structure stabilized by the template pattern. This is shown in Figure 1c,d.

The ability to design a template that introduces self-aligned pattern-free region between groups of lines coupled with the ability to deterministically truncate specific lines provides two useful tools to form images in the PMMA phase of the PS-*b*-PMMA BCP. The ability to achieve arbitrary grating-to-grating spacing using this method also relieves the restriction of having a universal single pitch grid as required for most chemical-epitaxy techniques. These images naturally lend themselves to the types of pattern constructs required to form fins in FinFET devices and circuits. However, the image formed after PMMA removal requires a tone inversion operation before it can be used to pattern the raised features required for fin patterning. An overview of the process we have developed is shown in Figure 2. In brief, the PMMA image is transferred into an organic planarizing layer (OPL) and a SiO_x-like film is spin-cast

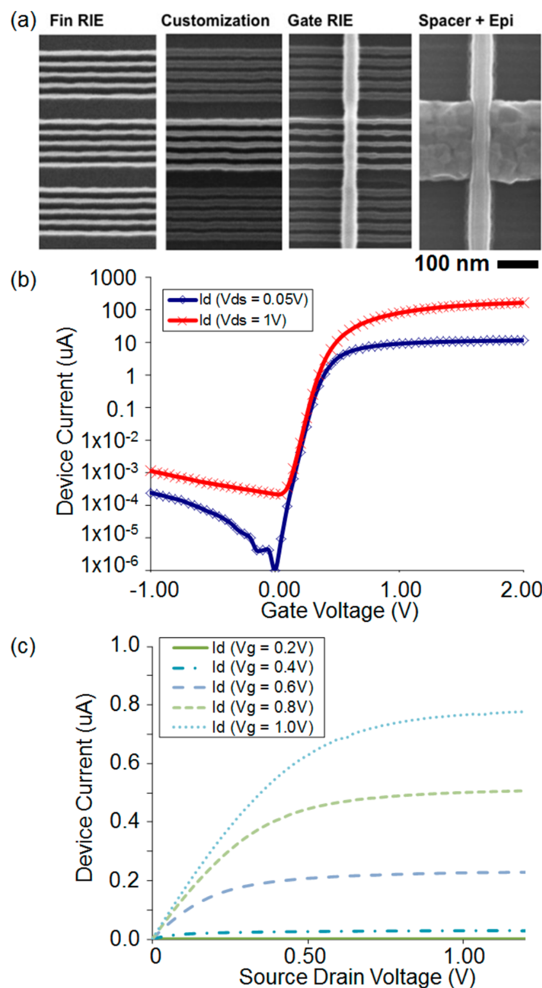


Figure 4. SOI devices with 29 nm-pitch fins fabricated using e-beam templated DSA lithography. (a) Using the process flow described in Figure 2a, groups of 5 fins were etched into SOI. A 193 nm lithography step is used to retain only the desired groups of SOI fins to form the active device. Because the edges of the 193 nm cut mask land in the regions generated by DSA templates, there is sufficient overlay budget and no partial fins are produced. A gate first process is then applied to form an isolated gate defined by e-beam lithography. After spacer formation, the finned source and drain are merged with a selective *in situ* phosphorus doped silicon epitaxial process. (b) Drain current *versus* gate voltage for a 5-fin FinFET device, demonstrating clear FET behavior with DSA patterned 29 nm-pitch fins. (c) Drain current *versus* source-drain voltage (Vds) for the same device. The flat drain current level at high Vds indicates good short channel DIBL control.

onto the wafers. A series of plasma etching processes are used which result in the creation of the PMMA image in the remaining SiO_x-like material. The tone-inverted image is then ultimately transferred into a 20 nm thin Si on insulator (SOI) layer using an additional plasma etch process to form groups of SOI fins. Figure 2b shows a top down SEM image of a group of fins formed using this process. Figure 2c shows a transmission electron microscope (TEM) image of the 29 nm pitch SOI fins.

Forming the fin patterns for more complicated circuit patterns requires the creation of fin-free regions

between blocks of adjacent fins. An example of this can be seen in a layout example of a FinFET logic circuit shown in Figure 3a.[9] In this example, 5 basic constructs are required to form the desired pattern (see Supporting Information for more details). The final fin pattern is accomplished through a combination of tone inverted graphoepitaxy to define the groups of fins and transverse cuts across entire groups of fins accomplished with an additional lithography step to form the fin-free regions. This additional patterning process creates an artifact of the removed fin in the underlying buried oxide layer (BOX), commonly referred to as BOX texturing (see Methods section for more details). Figure 3b shows the fin pattern of a 6 transistor (6T) static random access memory SRAM array and the corresponding DSA fins before and after the additional customization process.

Finally, in order to confirm the quality of such precustomized fins, we demonstrate the first functional DSA-patterned FinFET devices with 29 nm pitch SOI fins using a "gate first", high-k metal gate (HKMG) integration scheme (see Methods for more details). As shown in Figure 4a, groups of 5 fins were etched into SOI using the processes described in Figure 2a. A 193 nm lithography customization step then is used to retain only the desired groups of SOI fins to form the active device. The edges of the 193 nm customization pattern were designed to land in the pattern free regions generated by the DSA templates. This produces sufficient margin in the overlay budget to avoid the creation of partially removed fins. A "gate first" integration scheme, where the gate stack materials are first deposited over the entire wafer then patterned using subtractive patterning processes, is applied to form an isolated gate line. After spacer formation, the finned source and drain are merged with a selective *in situ* phosphorus doped silicon epitaxial process to provide source-drain doping and reduce external resistance. Figure 4b,c shows electrical measurements of a 5-fin device. The device $I-V$ curve shows reasonable on−off characteristics for a short channel device, such as an on−off ratio of 10^5, low drain induced barrier lowering (DIBL), and subthreshold slope of 70 mV/decade. Moreover, subthreshold slope and DIBL degradation associated with gross fin width variation was not observed.[10,11] These results confirmed that the graphoepitaxy-based DSA-pattern technique produces fins with sufficiently low variation and that a standard HKMG process can be exercised at 29 nm fin pitch. The on current can be further improved by optimizing junction formation, epitaxy formation, and silicide process, tasks that are beyond the scope of this work.

CONCLUSION

Line-space patterning with BCP DSA has been an active field of study for many years. Use of the DSA process to deterministically fabricate arbitrary circuit designs with nanoscale features remains as a major area of exploration. Combining previous efforts to improve the quality of pattern transfer[8] and the self-aligned customization scheme proposed in this paper, we demonstrated the first 29 nm pitch DSA-patterned FinFET devices with a standard semiconductor device fabrication process. Continued work to reduce linewidth and feature profile variation will further improve device performance. Advances on this front are anticipated through the use of improved BCP materials, advanced tone inversion materials, and state of the art pattern transfer techniques including advanced plasma etch reactors. While numerous reports on the defectivity of DSA-based patterning techniques have been published,[12] it is difficult to associate those studies with the work described in this publication. This form of DSA-based patterning will most likely require unique defectivity learning applied to a targeted patterning application.

METHODS

Experimental results in this study were conducted on full 200 mm wafers prepared using "production-style" semiconductor fabrication tools. The SOI device substrate is first coated with an OPL, which consists of a 30 nm amorphous carbon film deposited with chemical vapor deposition (CVD) at 550 °C. The hard mask material consists of 10 nm of plasma enhanced CVD (PECVD) SiN, deposited at 200 °C. Finally, a thin neutral layer[13] is spin-coated, annealed at 220 °C for 2 min, and rinsed to remove excess polymer brush before patterning of the DSA template and BCP coating. The template material used in this study was HSQ, a negative-tone electron-beam resist, patterned with electron beam lithography.[7] After HSQ development with TMAH, PS-*b*-PMMA BCP is coated and annealed at 250 °C for 2 min. The BCP used in this study is a 29 nm pitch PS-*b*-PMMA BCP from AZ Electronic Materials (AZ #18). The HSQ and BCP thicknesses are both 50 nm. All other aspects of the DSA process presented in this work are compatible with 193 nm immersion lithography processes.[13]

After forming the DSA patterns, an O_2-based plasma etching process is used for removing PMMA domains selectively from the BCP, and a CF_4-based etch process is used to transfer the remaining PS pattern into the hard mask layer. Following the hard mask etch, the pattern is transferred into the underlying OPL using an O_2-based plasma etch process. Fundamental studies on DSA based pattern transfer of FEOL materials are described elsewhere.[8,14] A tone-inversion process is then applied in the OPL layer by spin coating a spin-on dielectric material, IRM-007, from JSR Corporation, etching back to reveal the OPL, followed by removal of the OPL with a further O_2-based ashing. Note that the remaining hard mask layer on the surface of the OPL is consumed during the etch back of the dielectric material. This pattern is then transferred into a 10 nm thin layer of low pressure CVD silicon nitride. This layer is used as a hard mask for further patterning of the 20 nm thin SOI layer.

After fin formation, the fins regions are further defined with an additional customization process patterned by 193 nm lithography and plasma etching. This process is designed to remove fins selective to the BOX layer. However, texturing of the

BOX occurs leaving a faint artifact of the fin resulting from texturing of the BOX. This can be avoided through the incorporation of additional films and use of further plasma etch processes. In contrast, the fin-free regions created by the template pattern and adjacent BCP phases do not leave any residual pattern in the underlying BOX layer. A high-k metal gate stack is then deposited over the fins. The gate stack consists (from the bottom) of 2.2 nm of a hafnium-based dielectric, a 3 nm thin Ta-based electrode, a 30 nm thin amorphous silicon layer, and a 50 nm silicon nitride layer. Electron-beam lithography and plasma etching are used to define the gate pattern using procedures typical in a "gate first" FinFET integration scheme. This results in the removal of the gatestack materials from all areas of the substrate except the gate pattern regions. After gate formation, a self-aligned 10 nm silicon nitride spacer is formed by a novel spacer etch process with a ZEON Chemicals proprietary gas based chemistry, leaving spacer materials only on the gate sidewalls.[15] Finally, the device source, drain, and contact pads are merged with a selective *in situ* phosphorus doped silicon epitaxial process. A nickel silicide process is applied on the merged silicon pads to further reduce contact resistance.

Single chain in mean-field Monte Carlo simulations[16] were carried out to explore the effects of trench width, sidewall variation, and guide pattern wetting on the self-assembly process. Lamella-forming block copolymers were modeled as bead−spring chains with 20 beads each of PS and PMMA at a χN parameter of 16 k_BT and compressibility κ of 25 k_BT. Doi−Edwards bonds with an equilibrium length of 2.93 lattice units were used, making the bulk Rg of each chain approximately 7.5 lattice units. The bead number density was 21 beads per lattice cell. The equilibrium lamellar period of this model in a thin film is 28 lattice units, allowing a mapping of 1 lattice unit $\sim$1 nm. A variety of simulation volumes were explored, typically of the order 300 nm $\times$ 120 nm $\times$ 29 nm. Guiding pattern geometries were introduced to the system by a pair of static fields, a neutral field used to create excluded volumes like raised guide lines, and a selective field used to create an affinity between the simulated guide lines and the PMMA phase. The neutral field was also used to create an artificial "vapor" interface for the simulations of guide pattern wetting. The selective field favored contact with PMMA over PS by 2.0 k_BT. Each system was simulated for 5000 Monte Carlo sweeps, with 1 move/bead/sweep and mean-field updates after each sweep. The PS and PMMA densities from the final configurations were collected and visualized using OpenDX.[17] All calculations were carried out on an IBM BlueGene/P supercomputer at IBM Research, Almaden.

Conflict of Interest: The authors declare no competing financial interest.

Acknowledgment. The devices in this work were fabricated in the Microelectronics Research Laboratoy (MRL) at the IBM T. J. Watson Research Center. The authors are grateful to the MRL staff for their contributions to the success of this work. The authors would also like to thank I. Lauer, C.-H. Lin, L. Liebmann, G. Shahidi, and T.C. Chen for insightful discussions and their support.

Supporting Information Available: More detail and examples on the characteristics for FinFET logic circuits. This material is available free of charge *via* the Internet at http://pubs.acs.org.

REFERENCES AND NOTES

1. Auth, C.; Allen, C.; Blattner, A.; Bergstrom, D.; Brazier, M.; Bost, M.; Buehler, M.; Chikarmane, V.; Ghani, T.; Glassman, T.; *et al.* A 22nm High Performance and Low-Power CMOS Technology Featuring Fully-Depleted Tri-Gate Transistors, Self-Aligned Contacts and High Density MIM Capacitors. *VLSI Technol. Symp.* **2012**, 131–132.
2. Guillorn, M.; Chang, J.; Bryant, A.; Fuller, N.; Dokumaci, O.; Wang, X.; Newbury, J.; Babich, K.; Ott, J.; Haran, B.; *et al.* FinFET Performance Advantage at 22nm: An AC Perspective. *VLSI Technol. Symp.* **2008**, 12–13.
3. Hardy, C. M.; Bates, F. S.; Kim, M.-H.; Wignall, G. D. Model ABC Triblock Copolymers and Blends Near the Order-Disorder Transition. *Macromolecules* **2002**, *35*, 3189–3197.
4. Son, J. G.; Gotrik, K. W.; Ross, C. A. High-Aspect-Ratio Perpendicular Orientation of PS-*b*-PDMS Thin Films under Solvent Annealing. *ACS Macro Lett.* **2012**, *1*, 1279–1284.
5. Black, C. T. Self-Aligned Self Assembly of Multi-Nanowire Silicon Field Effect Transistors. *Appl. Phys. Lett.* **2005**, *87*, No. 163116.
6. Park, S. M.; Park, S. M.; Stoykovich, M. P.; Ruiz, R.; Zhang, Y.; Black, C. T.; Nealey, P. F. Directed Assembly of Lamellae-Forming Block Copolymers by Using Chemically and Topographically Patterned Substrates. *Adv. Mater.* **2007**, *19*, 607–611.
7. Yamaguchi, T.; Yamaguchi, H. Two-Dimensional Patterning of Flexible Designs with High Half-Pitch Resolution by Using Block Copolymer Lithography. *Adv. Mater.* **2008**, *20*, 1684–1689.
8. Tsai, H.; Miyazoe, H.; Engelmann, S.; To, B.; Sikorski, E.; Bucchignano, J.; Klaus, D.; Liu, C.-C.; Cheng, J.; Sanders, D.; *et al.* Sub-30nm Pitch Line-Space Patterning of Semiconductor and Dielectric Materials Using Directed Self-Assembly. *J. Vac. Sci. Technol., B: Microelectron. Nanometer Struct.—Process., Meas., Phenom.* **2012**, *30*, No. 06F205.
9. Vaidyanathan, K.; Ng, S. H.; Huang, W.; Morris, D.; Lafferty, N.; Liebmann, L.; Bender, M.; Huang, W.; Lai, K.; Pileggi, L.; Strojwas, A. Design and Manufacturability Tradeoffs in Unidirectional and Bidirectional Standard Cell Layouts in 14nm Node. *Proc. SPIE* **2012**, *8327*, No. 83270K.
10. Lin, C. H.; Haensch, W.; Oldiges, P.; Wang, H.; Williams, R.; Chang, J.; Guillorn, M.; Bryant, A.; Yamashita, T.; Standaert, T.; *et al.* Modeling of Width-Quantization-Induced Variations in Logic FinFETs for 22 nm and Beyond. *VLSI Technol. Symp.* **2011**, 16–17.
11. Yamashita, T.; Basker, V. S.; Standaert, T.; Yeh, C.-C.; Yamamoto, T.; Maitra, K.; Lin, C.-H.; Faltermeier, J.; Kanakasabapathy, S.; Wang, M.; *et al.* Sub-25 nm FinFET with Advanced Fin Formation and Short Channel Effect Engineering. *VLSI Technol. Symp.* **2011**, 14–15.
12. Takahashi, H.; Laachi, N.; Delaney, K. T.; Hur, S. M.; Weinheimer, C. J.; Shykind, D.; Fredrickson, G. H. Defectivity in Laterally Confined Lamella-Forming Diblock Copolymers: Thermodynamic and Kinetic Aspects. *Macromolecules* **2012**, *45*, 6253–6265.
13. Cheng, J. Y.; Sanders, D. P.; Truong, H. D.; Harrer, S.; Friz, A.; Holmes, S.; Colburn, M.; Hinsberg, W. D. Simple and Versatile Methods To Integrate Directed Self-Assembly with Optical Lithography Using a Polarity-Switched Photoresist. *ACS Nano* **2010**, *4*, 4815–4823.
14. Tsai, H.; Miyazoe, H.; Engelmann, S. U.; Liu, C.-C.; Gignac, L.; Bucchignano, J.; Klaus, D.; Breslin, C.; Joseph, E.; Cheng, J.; *et al.* Pattern Transfer of Directed Self-Assembly Patterns for CMOS Device Applications. *J. Micro/Nanolithogr., MEMS, MOEMS* **2013**, *12*, No. 041305.
15. Joseph, E. A.; Engelmann, S. U.; Miyazoe, H.; Bruce, R. L.; Nakamura, M.; Suzuki, T.; Hoinkis, M. Advanced Plasma Etch for the 10 nm Node and Beyond. *Proc. SPIE* **2013**, *8685*, No. 86850A.
16. Müller, M.; Smith, G. D. Phase Separation in Binary Mixtures Containing Polymers: A Quantitative Comparison of Single-Chain-In-Mean-Field Simulations and Computer Simulations of the Corresponding Multichain Systems. *J. Polym. Sci., Part B: Polym. Phys.* **2005**, *43*, 934–958.
17. OpenDX Web Page. www.opendx.org.